IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : GADDAM, et al.

Serial No. : 10/526,873

Confirmation No. : 7413

Filing Date : March 4, 2005

Group Art Unit : 2416

Examiner : Jamal Javaid

Attorney Docket No. : US020325

APPEAL BRIEF
On Appeal from Group Art Unit 2416

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed on June 4, 2009

and in response to the final Office action of March 4, 2009.

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I. REAL PARTY IN INTEREST

The real party in interest is Koninklijke Philips Electronics N.V., the assignee of record

as indicated at Reel/Frame 016983/0429.

II. RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any pending appeals, judicial proceedings, or interferences

which may be related to, directly affect, be directly affected by, or have a bearing on the Board's

decision in the pending appeal.

III. STATUS OF CLAIMS

a)   Claims 1-20 are pending at the time of filing the appeal brief.

b)   Claims 1 and 11 are independent.

c)   Claims 1-20 stand rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

The claims listed in section "VIII. Claims Appendix" of this Appeal Brief corresponds to

the claims as submitted in Appellants' amendment filed December 16, 2008. No claim

amendments have been submitted following the amendment of December 16, 2008, nor are any

amendments pending.

V. SUMMARY OF CLAIMED SUBJECT MATTER

It should be explicitly noted that it is not the Appellants' intention that the currently claimed or described embodiments be limited to operation within the illustrative embodiments described below beyond what is required by the claim language. Further description of the illustrative embodiments are provided indicating portions of the claims which cover the illustrative embodiments merely for compliance with requirements of this appeal without intending to read any further interpreted limitations into the claims as presented.

The claimed invention, as recited in claim 1, is directed to a digital signal transmission apparatus (page 5, lines 20-21) comprising: a multiplexer having an output port (page 5, line 23), an input port for inputting an information bit-stream and an input port for inputting a placeholder bit-stream (page 5, lines 23-25), for multiplexing the bit-streams inputted from the input ports to form a multiplexed bit-stream for output on the output port (page 5, line 25-page 6, line 2); a data formatter for receiving the multiplexed bit-stream and for replacing bits of said placeholder bit-stream within the received multiplexed bit-stream with bits derived from said information bit-stream within said received multiplexed bit-stream to form a modified bit-stream (page 6, lines 2-8); an encoder for encoding the modified bit-stream to produce an encoded bit-stream (page 6, lines 8-9); and a transmitter for transmitting the encoded bit-stream (page 6, lines 8-9).

The claimed invention, as recited in claim 11, is directed to a digital signal transmission method (page 5, lines 20-21) comprising: multiplexing an information bit-stream and a placeholder bit-stream to form a multiplexed bit-stream (page 5, line 25-page 6, line 2); receiving the multiplexed bit-stream (page 6, lines 3-4); replacing bits of said placeholder bit-stream within the received multiplexed bit-stream with bits derived from said information bit-stream within said received multiplexed bit-stream to form a modified bit-stream (page 6, lines 4-8); encoding

the modified bit-stream to produce an encoded bit-stream (page 6, lines 8-9); and transmitting

the encoded bit-stream (page 6, lines 8-9).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1, 2, 5-8, 10-12, 15-18, and 20 are properly rejected under 35 U.S.C. 103(a) as being unpatentable over Breti et al., US 2005/0152411 (hereinafter referred to as "Breti") in view of Bellier et al., US 2002/0194566 (hereinafter "Bellier").

B. Whether claims 3 and 13 are properly rejected under 35 U.S.C. 103(a) as being unpatentable over Breti in view of Bellier in further view of Abbott et al., US 6,438,569 (hereinafter "Abbott").

C. Whether claims 4 and 14 are properly rejected under 35 U.S.C. 103(a) as being unpatentable over Breti in view of Bellier in further view of Choi et al., US 2002/0041608 (hereinafter "Choi").

D. Whether claims 9 and 19 are properly rejected under 35 U.S.C. 103(a) as being unpatentable over Breti in view of Bellier in further view of Knutson et al., US 6,788,710 (hereinafter "Knutson").

VII. ARGUMENT

A. Claims 1, 2, 5-8, 10-12, 15-18, and 20 are not properly rejected under 35 U.S.C. 103(a) as being unpatentable over Breti in view of Bellier.

In re Wada and Murphy, Appeal 2007-3733, the BPAI stated that:

> "When determining whether a claim is obvious, an examiner must make "a searching comparison of the claimed invention – *including all its limitations* – with the teaching of the prior art." *In re Ochiai*, 71 F.3d 1565, 1572 (Fed. Cir. 1995) (emphasis added). Thus, "obviousness requires a suggestion of all limitations in a claim." *CFMT, Inc. v. Yieldup Intern. Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (*citing In re Royka*, 490 F.2d 981, 985 (CCPA 1974)). Moreover, as the Supreme Court recently stated, "*there must be some articulated reasoning* with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007) (quoting In re Kahn, 441 F.3d 977, 988 (Fed. Cir. 2006) (emphasis added))."

It is respectfully submitted that the Examiner failed to establish a *prima facie* case of obviousness, because as discussed below, a suggestion of all limitations in the claims is lacking in the combination of Breti and Bellier.

1. Claim 1

Appellants' independent claim 1 calls in part, for:

> . . . a multiplexer having an output port, an input port for inputting an information bit-stream and an input port for inputting a placeholder bit-stream, for multiplexing the bit-streams inputted from the input ports to form a multiplexed bit-stream for output on the output port;
> a data formatter for receiving the multiplexed bit-stream and for replacing bits of said placeholder bit-stream within the received multiplexed bit-stream with bits derived from said information bit-stream within said received multiplexed bit-stream to form a modified bit-stream. . .

In the Response to Arguments section at page 2, the final Office action suggests that the multiplexers 186 and 190 in figure 11 of Breti were newly taken together to collectively constitute the multiplexer of Appellants' claimed invention. The Office action alleges that this

manner of combining the two multiplexers constitutes one multiplexer, thereby suggesting Breti teaches that the replacing of the placeholder bit-stream is done with information bits within the same stream. Appellants disagree and respectfully submit that even if the multiplexers 186 and 190 of figure 11 of Breti are taken to collectively constitute the multiplexer of Appellants' claimed invention, Breti fails to suggest a data formatter for receiving the multiplexed bit-stream and for replacing bits of the placeholder bit-stream with bits derived from the same information bit-stream.

The Office action equates the elements 192 and 194 of Breti at figure 11 with the Appellants' claimed data formatter. Breti's data formatter (i.e. the combination of elements 192 and 194 of figure 11) receives two distinct multiplexed bit-streams; (1) the output of mux_2 186 and (2) the output of mux_1 190. This is in complete contrast with Appellants' claimed invention, which requires the data formatter to receive a multiplexed bit-stream and to replace bits from a placeholder bit-stream from within the multiplexed bit-stream with bits from the same information bit-stream.

The Office action's new interpretation at page 2 suggests that the two inputs to Breti's data formatter are the same information bit-stream. This is certainly not the case.

The first information bit-stream that is received by Breti's data formatter is clearly described in paragraph [0063] and figure 11. Encoders 162, 164, and 166 encode the uncoded auxiliary data by adding parity bits to the uncoded auxiliary data. The encoded auxiliary data are interleaved by interleavers 168, 170, and 172. Then the interleaved encoded uncoded auxiliary data are bitwise encoded by the outer coders 174, 176, and 178. The bitwise outputs of the outer coders are interleaved by small block interleavers 180, 182, and 184. The data outputs of the small block inverters 180, 182, and 184 are the data inputs to mux_2 186. Mux_2 186 selects

from among the inputs to mux_2 186. The output of mux_2 186 is the first information bit-stream that is received the data formatter.

The second information bit-stream that is received by Breti's data formatter is shown at figure 11, where mux_1 190 selects from among transport header, Advanced Television Systems Committee (ATSC) data, and ATSC Reed/Solomon parity bytes (referred to as [tx hdr dummy Rdata dummy ARSpar] data) information streams. The output of mux_1 190 is the second information bit-stream that is received by the data formatter. Unlike the information bit-stream from the output of mux_2 186, the information bit steam from the output of mux_1 190 was not encoded by adding parity bits, interleaved, bitwise encoded, and then interleaved. As such, the data formatter of Breti receives two separate and distinct multiplexed bit-streams. Therefore, Breti does not teach, disclose or even suggest replacing bits from a placeholder bit-stream from within the multiplexed bit-stream with bits from the same information bit-stream. Furthermore, Breti does not teach or suggest the data formatter to receive a multiplexed bit-stream.

The Office action at page 3 notes that Bellier is used only to teach replacing the bits of a placeholder bit-stream with information bits derived from the same data stream. The Office action alleges that Bellier essentially teaches this feature by inserting dummy bits into a coded block in pre-defined bit locations, interleaving, and then replacing dummy bits with bits indicative of signaling messages.

Appellants disagree and respectfully re-submit the argument as presented in the response dated December 16, 2008 that Bellier does not teach or suggest replacing the bits of a placeholder bit-stream with information bits derived from the same data stream.

Bellier appears to disclose a method of transmitting signaling messages by using the Slow Associated Control Channel (SACCH), wherein a plurality of dummy bits are inserted into

the SACCH block, and then the dummy bits in each SACCH block are replaced by the inband signaling for transmission. (Abstract). The Office action at page 3 apparently equates the SACCH block with the inband signaling and considers them to be the same data stream. This is clearly not the case.

Bellier apparently uses SACCH as a dedicated channel in a wireless telecommunications network for carrying information in blocks. Bellier at figure 1 and paragraph [0037] clearly discloses a method for the transmitting signaling messages in a SACCH block. At step 130, dummy bits are inserted into the SACCH block. At step 150, the dummy bits are replaced by bits representative of a signaling message. However, in complete contrast to Appellants' claimed invention, the SACCH block and the signaling message are clearly not derived from the same data stream. For example, in the last sentence of paragraph [0037], Bellier discloses that the signaling message can be derived from a Fast Power Control signal. As such, Bellier does not teach, disclose, or even suggest the feature of replacing bits of said placeholder bit-stream with bits derived from the same information bit-stream.

Because Breti and Bellier, separately or in combination, do not disclose or even suggest all limitations in the claimed invention, Appellants respectfully submit that the Office has not presented a prima facie case of obviousness and as such, the rejection to independent claim 1 under 35 U.S.C. 103(a), is unfounded and should be reversed.

2. Claim 11

Independent claim 11 includes similar features of: "replacing bits of said placeholder bit-stream within the received multiplexed bit-stream with bits derived from said information bit-stream within said received multiplexed bit-stream to form a modified bit-stream." Emphasis added. Appellants essentially repeat the above arguments from claim 1 and apply them to

independent claim 1 and for at least the same reasons as in claim 1, it is respectfully submitted that the rejection of claim 11, by Breti and Bellier, is not supported and the rejection should be reversed.

3. Claims 2, 5-8, 10, 12, 15-18, and 20

Claims 2, 5-8, 10, 12, 15-18, and 20 depend from claims 1 or 11 and incorporate by reference all of the features of the allowable parent claim.   Furthermore, each of these claims include additional distinguishing features. Appellants essentially repeat the above arguments from claim 1 or 11 and apply them to each of claims 2, 5-8, 10, 12, 15-18, and 20, respectively. As such, Appellants respectfully submit that claims 2, 5-8, 10, 12, 15-18, and 20 are allowable at least by virtue of their dependency on allowable base claims 1 or 11 and that the rejection under 35 U.S.C. 103(a), is unfounded and should be reversed.

B.   Claims 3 and 13 are not properly rejected under 35 U.S.C. 103(a) as being unpatentable over Breti in view of Bellier in further in view of Abbott.

4. Claims 3 and 13

Claims 3 and 13 ultimately depend from claim 1 or 11 and incorporate by reference all of the features of the allowable parent claim.   Furthermore, claims 3 and 13 each include additional distinguishing features. Appellants essentially repeat the above arguments from claims 1 or 11 and apply them to claims 3 and 13, respectively. Abbott does not cure the defects noted above as applied to claims 3 and 13.

Additionally, MPEP 2142 states:

> "[r]ejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."
> *In re Kahn*, 441 R.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).

> See also *KSR International Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741, 82
> USPQ2c 1385, 1396 (2007) (quoting Federal Circuit statement with
> approval).

The final Office action at the bottom of pages 14 and 15 simply provides a conclusory

statement that it would be obvious to one of ordinary skill in the art to modify Breti and Bellier

with the invention of Abbott. The Office does not provide any explanation or supporting

evidence as to why one of ordinary skill in the art would understand that such modification

would be motivated based on a system that is "fast, cost-effective, and reconfigurable."

The Office is simply providing conclusory statements to support the cited references in

making this rejection. Nowhere is there any suggestion in Breti, Bellier or Abbot, or with the

knowledge of one ordinarily skilled in the art to support these conclusory statements.

KSR makes clear that rejections on obviousness cannot be sustained by mere conclusory

statements; instead KSR requires that an Examiner provide "some articulated reasoning with

some rationale underpinning to support the legal conclusion of obviousness." (KSR Opinion at p.

14). An Examiner must "identify a reason that would have prompted a person of ordinary skill

in the relevant field to combine the elements in the way the claimed new invention does," (KSR

Opinion at p. 15). And, the Examiner must make "explicit" this rationale of "the apparent reason

to combine the known elements in the fashion claimed," including a detailed explanation of "the

effects of demands known to the design community or present in the marketplace" and "the

background knowledge possessed by a person having ordinary skill in the art." (KSR Opinion at

p. 14). Anything less than such an explicit analysis may not be sufficient to support a prima

facie case of obviousness. As such, Appellants respectfully submit that claims 3 and 13 are

allowable and that the rejection under 35 U.S.C. 103(a), is unfounded and should be reversed.

C. Claims 4 and 14 are not properly rejected under 35 U.S.C. 103(a) as being

unpatentable over Breti in view of Bellier in further view of Choi.

<u>5. Claims 4 and 14</u>

Claims 4 and 14 ultimately depend from claim 1 or 11 and incorporate by reference all of

the features of the allowable parent claim. Furthermore, claims 4 and 14 each include additional

distinguishing features. Appellants essentially repeat the above arguments from claims 1 or 11

and apply them to claims 4 and 14, respectively. Choi does not cure the defects noted above as

applied to claims 4 and 14. Additionally, the final Office action again makes conclusory

statements to support this combination without providing the proper support as discussed above

in subsection B. As such, Appellants respectfully submit that claims 4 and 14 are allowable at

least by virtue of their dependency on allowable base claims 1 or 11 and that the rejection under

35 U.S.C. 103(a), is unfounded and should be reversed.

D. Claims 9 and 19 are not properly rejected under 35 U.S.C. 103(a) as being

unpatentable over Breti in view of Bellier in further view of Knutson.

<u>6. Claims 9 and 19</u>

Claims 9 and 19 ultimately depend from claim 1 or 11 and incorporate by reference all of

the features of the allowable parent claim. Furthermore, claims 9 and 19 each include additional

distinguishing features. Appellants essentially repeat the above arguments from claims 1 or 11

and apply them to claims 9 and 19, respectively. Knutson does not cure the defects noted above

as applied to claims 9 and 19. Additionally, the final Office action again makes conclusory

statements to support this combination without providing the proper support as discussed above

in subsection B. As such, Appellants respectfully submit that claims 9 and 19 are allowable at

least by virtue of their dependency on allowable base claims 1 or 11 and that the rejection under

35 U.S.C. 103(a), is unfounded and should be reversed.

CONCLUSION

In light of the above, Appellants respectfully submit that the rejection of claims 1-20 is in

error, legally and factually, and must be reversed.

Respectfully submitted,

By: /Brian S. Myers/
    Brian S. Myers
    Attorney for Appellants
    Reg. No. 46,947
    973-401-7157

VIII. CLAIMS APPENDIX

1. (original) A digital signal transmission apparatus comprising:

a multiplexer having an output port, an input port for inputting an information bit-stream and an input port for inputting a placeholder bit-stream, for multiplexing the bit-streams inputted from the input ports to form a multiplexed bit-stream for output on the output port;

a data formatter for receiving the multiplexed bit-stream and for replacing bits of said placeholder bit-stream within the received multiplexed bit-stream with bits derived from said information bit-stream within said received multiplexed bit-stream to form a modified bit-stream;

an encoder for encoding the modified bit-stream to produce an encoded bit-stream; and

a transmitter for transmitting the encoded bit-stream.

2. (original)   The apparatus of claim 1, wherein the deriving creates a new bit, but retains any bit from which derivation has occurred.

3. (original)   The apparatus of claim 2, wherein said replacing comprises duplicating bits of said information bit-stream within said received multiplexed bit-stream to form duplicate bits and substituting the duplicate bits to replace bits of said placeholder bit-stream within said received multiplexed bit-stream.

4. (original)   The apparatus of claim 1, wherein the multiplexer is configured to multiplex an additional bit-stream in forming said multiplexed bit-stream, the data formatter is configured to bypass said replacing when operating on said additional bit-stream within said received multiplexed bit-stream to form said modified bit-stream, and the encoder is configured to process every bit of said modified bit-stream when operating on bits derived from said additional bit-stream and to process every other bit of said modified bit-stream when operating on bits derived from said information bit-stream.

5. (previously presented)   The apparatus of claim 1, wherein the multiplexer is configured with an additional input port for inputting an additional bit-stream.

6. (original)   The apparatus of claim 5, the multiplexer being configured to input a plurality of additional bit-streams, a plurality of information bit-streams and a plurality of placeholder bit-streams through their respective input ports for said multiplexing to form said multiplexed bit-stream, each of the information bit-streams to be multiplexed by the multiplexer having an identical number of bits, each of the placeholder bit-streams to be multiplexed by the multiplexer having an identical number of bits, the multiplexer being configured to multiplex each of the information and placeholder bit-streams for their respective identical number of bits before selecting another bit-stream for multiplexing.

7. (original)   The apparatus of claim 6, wherein said multiplexer is further configured to perform said multiplexing so as to select in succession, over a predetermined number of bit-streams, no more than three of said additional bit-streams.

8. (original)   The apparatus of claim 6 wherein said multiplexer is further configured to perform said multiplexing so as to input in succession one or more of the additional bit-streams after each input of one of an information bit-stream and a placeholder bit-stream.

9. (original)   The apparatus of claim 8, wherein the plural bit-streams are identical in length, and the inputting of one of an information bit-stream and a placeholder bit-stream successively alternates, over at least most inputs of the one information or placeholder bit-stream, between an information bit-stream and a placeholder bit-stream.

10. (original)   The apparatus of claim 1, wherein said replacing comprises removing selected bits from said information bit-stream within said received multiplexed bit-stream and substituting the removed bits to replace bits of said placeholder bit-stream within said received multiplexed bit-stream.

11. (previously presented) A digital signal transmission method comprising:

multiplexing an information bit-stream and a placeholder bit-stream to form a multiplexed bit-stream;

receiving the multiplexed bit-stream;

replacing bits of said placeholder bit-stream within the received multiplexed bit-stream with bits derived from said information bit-stream within said received multiplexed bit-stream to form a modified bit-stream;

encoding the modified bit-stream to produce an encoded bit-stream; and

transmitting the encoded bit-stream.

12. (original) The method of claim 11, wherein the deriving creates a new bit, but retains any bit from which derivation has occurred.

13. (previously presented)   The method of claim 12, wherein the replacing comprises:

duplicating bits of said information bit-stream within said received multiplexed bit-stream to form duplicate bits; and

substituting the duplicate bits to replace bits of said placeholder bit-stream within said received multiplexed bit-stream.

14. (previously presented)   The method of claim 11, further comprising:

multiplexing an additional bit-stream in forming said multiplexed bit-stream; and

bypassing said replacing step when operating on said additional bit-stream within said received multiplexed bit-stream to form said modified bit-stream;

wherein said encoding further comprises:

processing every bit of said modified bit-stream when operating on bits derived from said additional bit-stream; and

processing every other bit of said modified bit-stream when operating on bits derived from said information bit-stream.

15. (previously presented)   The method of claim 11, wherein the multiplexing further comprises multiplexing an additional bit-stream to form said multiplexed bit-stream.

16. (previously presented)   The method of claim 15, wherein said multiplexing comprises multiplexing a plurality of additional bit-streams, a plurality of information bit-streams, and a plurality of placeholder bit-streams to form said multiplexed bit-stream, each of said information

bit-streams to be multiplexed by the multiplexer having an identical number of bits, each of said placeholder bit-streams to be multiplexed by the multiplexer having an identical number of bits, the multiplexing step being performed so as to multiplex each of the information and placeholder bit-streams for their respective identical number of bits before selecting another bit-stream for multiplexing.

17. (previously presented)   The method of claim 16, wherein said multiplexing is performed so as to select in succession, over a predetermined number of bit-streams, no more than three of said additional bit-streams.

18. (previously presented)   The method of claim 16 wherein the multiplexing multiplexes so as to input in succession one or more of the additional bit-streams after each input of one of an information bit-stream and a placeholder bit-stream.

19. (original)   The method of claim 18, wherein the plural bit-streams are identical in length, and the inputting of one of an information bit-stream and a placeholder bit-stream successively alternates, over at least most inputs of the one information or placeholder bit-stream, between an information bit-stream and a placeholder bit-stream.

20. (previously presented)   The method of claim 11, wherein the replacing comprises:

    selecting bits from said information bit-stream within said received multiplexed bit-stream;

    removing the selected bits from said information bit-stream within said multiplexed bit-stream; and

    substituting the removed bits to replace bits of said placeholder bit-stream within said received multiplexed bit-stream.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title nor any

other evidence entered by the examiner and relied upon by Appellants in the appeal.

X. RELATED PROCEEDINGS APPENDIX

Appellants are not aware of any appeals or interferences related to the present

application.